a sixth switching MOS transistor having a source-drain path provided between the other of said pair of data lines and said terminal being supplied with said intermediate level potential,

wherein said fifth and sixth switching MOS transistors set said pair of data lines at said intermediate level when said plurality of memory cells are in said non-selected state. --

REMARKS

Entry of this Amendment in accordance with the provisions of 37 CFR 1.312 is respectfully requested.

By the present Amendment, it is requested that new dependent claim 25 be added in this case. New claim 25 depends on claim 24, and defines additional transistors for the overall circuit. Specifically, claims 20-24 define first through fourth switching MOS transistors. Claim 25 adds to this by defining a fifth and a sixth MOS switching transistor. With regard to this, it is noted that clear antecedent support exists for the language of claim 25 in its parent claims. Specifically, as noted above, first through fourth switching MOS transistors are already defined, so that no antecedent basis or numbering problems exist concerning the addition of "a fifth switching MOS transistor" and "a sixth switching MOS transistor." Also, antecedent basis is established for "said pair of data lines" in claim 1. In addition, antecedent basis